

WHAT IS CLAIMED IS:

1. A system for enabling facilitated analysis of malfunction on a PCI bus, arranged in a computer device in which a processor unit is connected over the PCI bus to a plural number of PCI devices, said system comprising:

5 said plural PCI devices, each of which, when operating as a PCI target device, activates a corresponding target operating signal; and

a PCI bus monitor circuit for monitoring target address of a command executed on said PCI bus and said target operating signals from said plural PCI devices, said PCI bus monitor circuit sending an error report signal to said processor unit when plural PCI target devices
10 respond for one PCI cycle.

2. The system as defined in claim 1 wherein said PCI bus monitor circuit includes:

an address storage circuit for snooping the operation of said PCI bus at the time of booting said computer device to store base address values and size values of said plural PCI devices in association with the
5 target operating signals;

an address latch circuit for storing temporarily the target address on said PCI bus;

a target device selection circuit for specifying the PCI target
10 device based on the base address values and size values of the plural PCI devices stored in said address storage circuit and on the target address temporarily stored in said address latch circuit;

a target comparator circuit for comparing a result of said target

device selection circuit and states of said target operating signals and
 15 for detecting that plural PCI target devices have responded for one PCI
 cycle; and

an error status circuit for storing the result of said target device
 selection circuit and plural target operating signals from said target
 comparator circuit activated for one PCI cycle to report to said
 20 processor unit that plural PCI target devices have responded for one PCI
 cycle by way of the error report signal.

3. The system as defined in claim 1 wherein said PCI bus monitor
 circuit includes:

an address storage circuit, in which base address values and size
 values of said plural PCI devices in association with the target operation
 5 signals are stored by the processor unit at the time of booting said
 computer device;

an address latch circuit for storing temporarily the target address
 on said PCI bus;

a target device selection circuit for specifying the PCI target
 10 device based on the base address values and size values of the plural PCI
 devices stored in said address storage circuit and on the target address
 temporarily stored in said address latch circuit;

a target comparator circuit for comparing a result of the target
 device selection circuit and states of said target operating signals and
 15 for detecting that plural PCI target devices have responded for one PCI
 cycle; and

an error status circuit for storing the result of said target device

selection circuit and plural target operating signals from said target comparator circuit activated for one PCI cycle to report to said processor unit that plural PCI target devices have responded for one PCI cycle by way of the error report signal.

4. A system for enabling facilitated analysis of malfunction on a PCI bus, arranged in a computer device in which a processor unit is connected over the PCI bus to a plural number of PCI devices, said system comprising:

5 said plural PCI devices, each of which, when operating as a PCI target device, activates corresponding target operating signal; and

a PCI bus monitor circuit for monitoring target address of a command executed on said PCI bus and said target operating signals from said plural PCI devices, said PCI bus monitor circuit including means for resetting said PCI bus when plural PCI target devices respond for one PCI cycle.

5. The system as defined in claim 4 wherein said PCI bus monitor circuit includes:

an address storage circuit for snooping the operation of said PCI bus at the time of booting said computer device to store base address values and size values of said plural PCI devices in association with the target operating signals;

an address latch circuit for storing temporarily the target address on said PCI bus;

a target device selection circuit for specifying the PCI target device based on the base address values and size values of the plural PCI

devices stored in said address storage circuit and on the target address temporarily stored in said address latch circuit;

15 a target comparator circuit for comparing a result of said target device selection circuit and states of said target operating signals and for detecting that plural PCI target devices have responded for one PCI cycle;

 an error status circuit for storing the result of said target device selection circuit and plural target operating signals from said target comparator circuit activated for one PCI cycle; and

20 a PCI reset generating circuit for executing reset operation of said PCI bus with contents of said error status circuit being held by the PCI reset generating circuit to reset all of the PCI devices connected to said PCI bus.

6. The system as defined in claim 4 wherein said PCI bus monitor circuit includes:

5 an address storage circuit, in which base address values and size values of said plural PCI devices in association with the target operation signals are stored by the processor unit at the time of booting said computer device;

 an address latch circuit for storing temporarily the target address on said PCI bus;

10 a target device selection circuit for specifying the PCI target device based on the base address values and size values of the plural PCI devices stored in said address storage circuit and on the target address temporarily stored in said address latch circuit;

a target comparator circuit for comparing a result of the target device selection circuit and states of said target operating signals and
 15 for detecting that plural PCI target devices have responded for one PCI cycle;

an error status circuit for storing the result of said target device selection circuit and plural target operating signals from said target comparator circuit activated for one PCI cycle; and

20 a PCI reset generating circuit for executing reset operation of said PCI bus with contents of said error status circuit being held by the PCI reset generating circuit to reset all of the PCI devices connected to said PCI bus.

7. A system for enabling facilitated analysis of malfunction on a PCI bus arranged in a computer device in which a processor unit is connected over the PCI bus to a plural number of PCI devices, said system comprising:

5 said processor unit activating corresponding target operating signal when operating as a PCI target device;

said plural PCI devices, each of which, when operating as a PCI target device, activates corresponding target operating signal; and

a PCI bus monitor circuit for monitoring target address of a
 10 command executed on said PCI bus and the target operating signals from said processor unit and from said plural PCI devices, said PCI bus monitor circuit sending an error report signal to said processor unit when plural PCI target devices have responded for one PCI cycle.

8. The system as defined in claim 7 wherein said PCI bus monitor

circuit includes:

an address storage circuit for snooping the operation of said PCI bus at the time of booting said computer device to store base address values and size values of said plural PCI devices in association with the target operating signals;

an address latch circuit for storing temporarily the target address on said PCI bus;

a target device selection circuit for specifying the PCI target device based on the base address values and size values of the plural PCI devices stored in said address storage circuit and on the target address temporarily stored in said address latch circuit;

a target comparator circuit for comparing a result of said target device selection circuit and states of said target operating signals and for detecting that plural PCI target devices have responded for one PCI cycle; and

an error status circuit for storing the result of said target device selection circuit and plural target operating signals from said target comparator circuit activated for one PCI cycle to report to said processor unit that plural PCI target devices have responded for one PCI cycle by way of the error report signal.

9. The system as defined in claim 7 wherein said PCI bus monitor circuit includes:

an address storage circuit, in which base address values and size values of said plural PCI devices in association with the target operation signals are stored by the processor unit at the time of booting said

computer device;

an address latch circuit for storing temporarily the target address on said PCI bus;

a target device selection circuit for specifying the PCI target device based on the base address values and size values of the plural PCI devices stored in said address storage circuit and on the target address temporarily stored in said address latch circuit;

a target comparator circuit for comparing the result of said target device selection circuit and states of said target operating signals and for detecting that plural PCI target devices have responded for one PCI cycle; and

an error status circuit for storing the result of said target device selection circuit and plural target operating signals activated for one PCI cycle to report to said processor unit that plural PCI target devices have responded for one PCI cycle by way of the error report signal.

10. A system for enabling facilitated analysis of malfunction on a PCI bus, arranged in a computer device in which a processor unit is connected over the PCI bus to a plural number of PCI devices, said system comprising:

said processor unit activating corresponding target-operating signal, when operating as a PCI target device;

said plural PCI devices, each of which, when operating as a PCI target device, activates corresponding target-operating signal; and

a PCI bus monitor circuit for monitoring target address of a command executed on said PCI bus and said target operating signals

from said plural PCI devices, said PCI bus monitor circuit including means for resetting said PCI bus when plural PCI target devices respond for one PCI cycle.

11. The system as defined in claim 10 wherein said PCI bus monitor circuit includes:

an address storage circuit for snooping the operation of said PCI bus at the time of booting said computer device to store base address values and size values of said plural PCI devices in association with the target operating signals;

an address latch circuit for storing temporarily the target address on said PCI bus;

a target device selection circuit for specifying the PCI target device based on the base address values and size values of said processor unit and the plural PCI devices stored in said address storage circuit and on the target address temporarily stored in said address latch circuit;

a target comparator circuit for comparing a result of said target device selection circuit and states of said target operating signals and for detecting that plural PCI target devices have responded for one PCI cycle;

an error status circuit for storing the result of said target device selection circuit and plural target operating signals from said target comparator circuit activated for one PCI cycle; and

a PCI reset generating circuit for executing reset operation of said PCI bus with contents of said error status circuit being held by the PCI

reset generating circuit to reset all of the PCI devices connected to said PCI bus.

12. The system as defined in claim 10 wherein said PCI bus monitor circuit includes:

an address storage circuit, in which base address values and size values of said plural PCI devices in association with the target operation
5 signals are stored by the processor unit at the time of booting said computer device;

an address latch circuit for storing temporarily the target address on said PCI bus;

a target device selection circuit for specifying the PCI target
10 device based on the base address values and size values of said processor unit and the plural PCI devices stored in said address storage circuit and on the target address temporarily stored in said address latch circuit;

a target comparator circuit for comparing the result of the target
15 device selection circuit and states of said target operating signals and for detecting that plural PCI target devices have responded for one PCI cycle;

an error status circuit for storing the result of said target device selection circuit and plural target operating signals from said target
20 comparator circuit activated for one PCI cycle; and

a PCI reset generating circuit for executing reset operation of said PCI bus with contents of said error status circuit held by the PCI reset generating circuit to reset all of the PCI devices connected to said PCI

bus.

13. The system as defined in claim 7 wherein

said processor unit includes a micro-processor, a host bridge and a memory and wherein

said target operating signal is sent from said host bridge to said

5 PCI bus monitor circuit.

14. The system as defined in claim 10 wherein

said processor unit includes a micro-processor, a host bridge and a memory and wherein

said target operating signal is sent from said host bridge to said PCI bus monitor circuit.